remains at the corners to prevent the diffusion of copper (110) and to provide sufficient amount of conductivity during the ECD process (112).

By performing a sputter etch after the liner/barrier deposition instead of before it, the oxide re-deposition from the sidewalls of the via/trench onto the bottom of the via/trench is eliminated. Because it is the liner/barrier/seed material that is sputter etched, only liner/barrier/seed (metal) material is redeposited at the bottom of the trench/via. Redeposition of the metal does not result in high interfacial resistance as does redeposition of oxide material because of materials conductivity difference.

After the sputter etch, copper ECD is performed as shown in FIG. 2D to form copper layer 124. Because the sputter etch removes/reduces the overhang 111, no seam forms in electroplated copper layer 124 due to early closure at the tops of the trench or via. Various copper ECD processes are known in the art. In one example, a 3-step process is used. After placing the wafer in the plating solution, a current of approximately 0.75 Amps is passed through the seed layer 112 for a time on the order of 15 secs. The current is then increased to around 3 Amps for approximately 60 seconds. Final plating occurs at a current of about 7.5Amps with the duration determined by the final desired thickness. A quick spin-rinse dry (SRD) is performed in the plating cell above the plating solution. The wafer is then transferred to the SRD cell and a post-ECD SRD is used to clean the plating residue.

Processing then continues to chemically-mechanically polish the copper layer 124 and liner/barrier 110 to form the copper interconnect, as shown in FIG. 2E. Additional metal interconnect layers may then be formed followed by packaging.

A second embodiment of the invention will now be discussed in conjunction with a process for forming a tungsten contact. Referring to FIG. 3A, a semiconductor body 200 is processed through the formation of the pre-metal dielectric (PMD) 210. Semiconductor body 200 has transistors (source/drains 202, gate dielectric 204, gate electrode 206) formed therein. Contact holes 212 are etched in PMD 210 to make contact to, for example, source/drain 202.

Referring to FIG. 3B, a liner/barrier 214 is deposited over PMD 210 using a PVD process. Liner/barrier 214 may comprise Ti. Because a PVD process is used, the portion of the liner/barrier material at the top edges of contact hole 212 is thicker and creates overhang 216.

After deposition of liner/barrier 214, a light sputter etch is performed to reduce or remove overhang 216, as shown in FIG. 3C. The sputter etch uses a low bias to improve the film profile. By using a low bias, only the liner/barrier metal in the field and top corners is removed. The bottom film thickness does not change significantly and therefore, the amount of material at the bottom interface is preserved. The sputter etch is preferably performed in situ after the liner/barrier deposition without breaking vacuum to preserve the film's integrity.

By performing a sputter etch after the liner/barrier deposition instead of before it, the oxide re-deposition from the sidewalls of the contact onto the bottom of the contact is eliminated. Because it is the liner/barrier metal that is sputter etched, only liner/barrier metal is redeposited at the bottom of the contact. Redeposition of the metal does not result in high interfacial resistance as does redeposition of oxide material.

After the sputter etch, a barrier layer 218 such as CVD/PVD TiN is deposited followed by the fill material 220. The fill material 220 and liner/barrier layer 214/218 are then chemically-mechanically polished to form a conductive

plug 222, as shown in FIG. 3D. The fill material 220 typically comprises tungsten or alternative material such as CVD TiN. An overhang of the liner/barrier material 214 can cause a seam to form in the fill material 220. Because overhang 216 has been reduced or removed, seam formation is minimized in the fill material 220.

Processing then continues with the formation of metal interconnects and packaging.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.